

Objectives:

- Learn basic Makefile use.

Exercise:

Open a unix terminal (either in Linux or by using PuTTY).

The basic Makefile syntax is as follows:

```
target: prereq1 prereq2
    commands
```

For example,

```
foo.o: foo.c foo.h
    gcc -c foo.c
```

The target is always a file...unless it's in the ".PHONY:" list. For example, if there was a "make all" target, you must have ".PHONY: all" in the Makefile. You may also have variables in your Makefile. For example, you may have "CC=gcc". Then you could say "\$(CC) foo.c" in the commands portion of your Makefile targets.

For this exercise you will need to create a Makefile for the project downloaded.

Add targets for "lab4.o" and "lab4". I should be able to run "make lab4" and have a "lab4" executable. "make test" should run lab4 after a "make clean" is issued.